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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,183	04/02/2001	David S. Christie	5500-66100	1668

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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,183	CHRISTIE ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004 and 03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/28/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 31-60 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Request to Rescind Previous Non-Publication Request as received on 7/30/01, IDS as received on 4/28/04 and Amendment A as received on 5/03/04.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations that a peripheral device be a modem as in claim 47, a network interface device as in claim 48, and an audio device as in claim 50, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The

replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 52-53 and 57-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 52 recites the limitation, "a least significant portion of a different one of the plurality of registers". It is unclear from the claim language what this "different one of the plurality of registers" is different from. Please clarify the claim language to more clearly define

the metes and bounds of the claim. Claim 57 also recites the same limitation, and thus requires similar clarification. Dependent claims 53 and 58 contain all of the limitations of their parent claims, and thus are rejected for the same reasons as above.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 31-42 and 51-60 are rejected under 35 U.S.C. 102(b) as being anticipated by Turley, *Advanced 80386 Programming Techniques* (hereinafter Turley).

11. Regarding claims 31, 35 and 39, taking claim 35 as exemplary, Turley has taught an apparatus comprising:

a. One or more storage locations corresponding to a plurality of registers (Fig. 1-5, see p.19-20),

b. A processor (80386 on p.263) coupled to the one or more storage locations (see p.263), wherein the processor, responsive to an instruction having a register address field (see p.263), is configured to:

I. Map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field (see p.263-264). Here, when an instruction that is to operate on 32 bit registers contains the operand-size override prefix byte, it maps

the register address field to the least significant portion (lower 16 bits) of any of the registers (see AX portion of EAX on p.262 and AX, BX, CX, DX examples on p.263).

II Map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field (see p.263-264). Here, when an instruction that is to operate on 32 bit registers does not contain the operand-size override prefix byte, it maps the register address field to the least significant portion (second lowest 16 bits) of a subset of the registers, specifically any of the 32-bit registers (see EAX example on p.262 and p.263-264).

12. Claims 31 and 39 are nearly identical to claim 35. Claim 31 differs in its lack of an apparatus, and claim 39 differs in its being comprised within a method, but both claims 31 and 39 encompass the same scope as claim 35. Therefore, claims 31 and 39 are rejected for the same reasons as claim 35.

13. Regarding claims 32, 36 and 40, taking claim 36 as exemplary, Turley has taught the apparatus as recited in claim 35, wherein the prefix field is a prefix byte (see p.263 lines 1-7).

14. Claims 32 and 40 are nearly identical to claim 36, differing in their parent claims, but encompassing the same scope as claim 36. Therefore, claims 32 and 40 are rejected for the same reasons as claim 36.

15. Regarding claims 33, 37 and 41, taking claim 37 as exemplary, Turley has taught the apparatus as recited in claim 35, wherein the instruction specifies a one byte operand size (see

p.263). Here, because the operand-size override prefix byte does not affect instructions that include one byte operands, and instruction can specify a one byte operand and the operand-size override prefix byte causing a mapping to a least significant (lower 8 bits) of any of the registers to be created.

16. Claims 33 and 41 are nearly identical to claim 37, differing in their parent claims, but encompassing the same scope as claim 37. Therefore, claims 33 and 41 are rejected for the same reasons as claim 37.

17. Regarding claims 34, 38 and 42, taking claim 38 as exemplary, Turley has taught the processor as recited in claim 37, wherein the least significant portion and the second least significant portion each comprise a byte (see p.263-264). Here, 16 bits "comprises" one byte, and thus Turley has taught the least significant portion and the second least significant portion "comprising" a byte.

18. Claims 34 and 42 are nearly identical to claim 38, differing in their parent claims, but encompassing the same scope as claim 38. Therefore, claims 34 and 42 are rejected for the same reasons as claim 38.

19. Regarding claims 51 and 56, taking claim 56 as exemplary, Turley has taught an apparatus comprising:

a. One or more storage locations corresponding to a plurality of registers (Fig. 1-5, see p.19-20),

b. A processor (80386 on p.263) coupled to the one or more storage locations (see p.263), wherein the processor is configured responsive to an instruction having a register address field (see p.263), to:

I. Utilize a first mapping of values of the register address field to the plurality of registers as a selected mapping responsive to the instruction including a prefix field (see p.263-264). Here, when an instruction that is to operate on 32 bit registers contains the operand-size override prefix byte, it maps the register address field to the least significant portion (lower 16 bits) of any of the registers (see AX portion of EAX on p.262 and AX, BX, CX, DX examples on p.263).

II. Utilize a second mapping of values of the register address field to the plurality of registers as the selected mapping responsive to the instruction excluding the prefix field (see p.263-264). Here, when an instruction that is to operate on 32 bit registers does not contain the operand-size override prefix byte, it maps the register address field to the least significant portion (second lowest 16 bits) of a subset of the registers, specifically any of the 32-bit registers (see EAX example on p.262 and p.263-264).

III. Wherein the processor is configured to select one of the plurality of registers responsive to a value of the register address field and the selected mapping (see p.262-264). Here, the operand-size override prefix byte specifies the which mapping the instruction is to use, and based on that the instruction accesses the appropriate register using the selected mapping.

20. Claim 51 is nearly identical to claim 56. Claim 51 differs in its lack of an apparatus, but encompasses the same scope as claim 56. Therefore, claim 51 is rejected for the same reasons as claim 56.

21. Regarding claims 52 and 57, taking claim 57 as exemplary, Turley has taught the apparatus as recited in claim 56, wherein the first mapping maps each value of the register address field to a least significant portion of a different one of the plurality of registers (see above paragraph XX and p.263-264). Here, when an instruction that is to operate on 32 bit registers contains the operand-size override prefix byte, it maps the value of the register address field to the least significant portion (lower 16 bits) of any of the registers (see AX, BX, CX, DX examples on p.263), any of which is a different register than the 32 bit registers that the instruction would be require to map to if the prefix byte is absent.

22. Claim 52 is nearly identical to claim 57, differing in its parent claim, but encompassing the same scope as claim 57. Therefore, claim 52 is rejected for the same reasons as claim 57.

23. Regarding claims 53 and 58, taking claim 58 as exemplary, Turley has taught the apparatus as recited in claim 57, wherein the second mapping maps each value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers (see p.263-264). Here, when an instruction that is to operate on 32 bit registers does not contain the operand-size override prefix byte, it maps the value of the register address field to the least significant portion (second lowest 16 bits) of a subset of the registers, specifically any of the 32-bit registers (see EAX example on p.262 and p.263-264).

24. Claim 53 is nearly identical to claim 58, differing in its parent claim, but encompassing the same scope as claim 58. Therefore, claim 53 is rejected for the same reasons as claim 58.

25. Regarding claims 54 and 59, taking claim 59 as exemplary, Turley has taught the apparatus as recited in claim 56, wherein the prefix field is a prefix byte (see p.263 lines 1-7).

26. Claim 54 is nearly identical to claim 59, differing in its parent claim, but encompassing the same scope as claim 59. Therefore, claim 54 is rejected for the same reasons as claim 59.

27. Regarding claims 55 and 60, taking claim 60 as exemplary, Turley has taught the apparatus as recited in claim 56, wherein the instruction specifies a one byte operand size (see p.263). Here, because the operand-size override prefix byte does not affect instructions that include one byte operands, and instruction can specify a one byte operand and the operand-size override prefix byte causing a mapping to a least significant (lower 8 bits) of any of the registers to be created.

28. Claim 55 is nearly identical to claim 60, differing in its parent claim, but encompassing the same scope as claim 60. Therefore, claim 55 is rejected for the same reasons as claim 60.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 43-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turley, *Advanced 80386 Programming Techniques* (hereinafter Turley), in further view of Gulick et al., U.S. Patent No. 5,732,224.

31. Regarding claim 43, Turley has taught a computer system comprising:

a. A processor (80386 on p.263) comprising a register file including a plurality of registers (Fig. 1-5, see p.19-20), wherein the processor, responsive to an instruction having a register address field (see p.263), is configured to:

I. Map a value of the register address field to a last significant portion of one of the plurality of registers responsive to the instruction including a prefix field (see p.263-264). Here, when an instruction that is to operate on 32 bit registers contains the operand-size override prefix byte, it maps the register address field to the least significant portion (lower 16 bits) of any of the registers (see AX portion of EAX on p.262 and AX, BX, CX, DX examples on p.263).

II. Map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field (see p.263-264). Here, when an instruction that is to operate on 32 bit registers does not contain the operand-size override prefix byte, it maps the register address field to the least significant portion (second lowest 16 bits) of a subset of the registers, specifically any of the 32-bit registers (see EAX example on p.262 and p.263-264).

32. Turley has not explicitly taught wherein the computer system further comprises a peripheral device configured to communicate between the computer system and another computer system.

33. However, Gulick has taught that conventional computer systems contain a processor, as well as various peripherals coupled to the processor, such as network interface cards, modems and audio devices (see Gulick, Col.1 lines 17-34), so that the systems' functionality can be expanded to include real-time applications (see Gulick, Col.1 lines 35-45). Because it is desirable for a microprocessor to have its functionality expanded by incorporating it into a system, and further because such an expansion is conventionally performed, one of ordinary skill in the art would have found it obvious to modify the processing system of Turley to include multiple peripheral devices such as a NIC, modem, or audio device, so that the system's functionality can be enhanced per conventional techniques.

34. Regarding claim 44, Turley in view of Gulick has taught the computer system as recited in claim 43, wherein the prefix field is a prefix byte (see Turley, p.263 lines 1-7).

35. Regarding claim 45, Turley in view of Gulick has taught the computer system as recited in claim 43, wherein the instruction specifies a one byte operand size (see Turley, p.263). Here, because the operand-size override prefix byte does not affect instructions that include one byte operands, and instruction can specify a one byte operand and the operand-size override prefix byte causing a mapping to a least significant (lower 8 bits) of any of the registers to be created.

36. Regarding claim 46, Turley in view of Gulick has taught the computer system as recited in claim 43, wherein the least significant portion and the second least significant portion each comprise a byte (see Turley, p.263-264). Here, 16 bits "comprises" one byte, and thus Turley has taught the least significant portion and the second least significant portion "comprising" a byte.

37. Regarding claim 47, Turley in view of Gulick has taught the computer system as recited in claim 43, wherein the peripheral device comprises a modem (see Gulick, Col.1 lines 17-34, as well as above paragraphs 28-30).

38. Regarding claim 48, Turley in view of Gulick has taught the computer system as recited in claim 43, wherein the peripheral device comprises a network interface device (see Gulick, Col.1 lines 17-34, as well as above paragraphs 28-30).

39. Regarding claim 49, Turley in view of Gulick has taught the computer system as recited in claim 43, but has not explicitly taught wherein the system further comprises a second processor comprising a register file including a plurality of registers, wherein the second processor, responsive to an instruction having a register address field, is configured to:

I. Map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field,

II. Map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field.

40. While Turley has taught a single processor comprising all of the limitations of claim 49 (see above paragraphs 28-30), Turley has not explicitly taught a second processor comprising those same limitations. However, the inclusion of a second processor with no reference in the claims as to how it is configured in relation to the first processor provides no new or unexpected result over the prior art of record. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the processor, creating a second processor comprising all of the limitations

of the first processor of Turley (see In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

41. Regarding claim 50, Turley in view of Gulick has taught the computer system as recited in claim 43, further comprising an audio device (see Gulick, Col.1 lines 17-34, as well as above paragraphs 28-30).

Response to Arguments

42. Applicant's arguments with respect to claims 31-60 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

46. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
8/6/2004

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